SYSTEMS AND METHODS FOR REDUCING STATIC AND TOTAL POWER CONSUMPTION IN PROGRAMMABLE LOGIC DEVICE ARCHITECTURES

Abstract of the Invention

[0087] A method and system for reducing power consumption in a programmable logic device (PLD) is provided. The power consumption may be reduced by preferably continually considering power consumption as a factor in circuit design during the synthesis, placement, routing, and period following routing of the programmable logic device.